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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/085,782	02/28/2002	Yueyong Wang	RAMB-01009US0	2045
28554	7590	03/11/2004	EXAMINER	
VIERRA MAGEN MARCUS HARMON & DENIRO LLP 685 MARKET STREET, SUITE 540 SAN FRANCISCO, CA 94105				NGUYEN, MINH T
ART UNIT		PAPER NUMBER		
2816				

DATE MAILED: 03/11/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	<b>Application No.</b>	<b>Applicant(s)</b>
	10/085,782	WANG ET AL.
	<b>Examiner</b>	<b>Art Unit</b>
	Minh Nguyen	2816

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

#### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1) Responsive to communication(s) filed on 11 February 2004.  
 2a) This action is FINAL.                    2b) This action is non-final.  
 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) Claim(s) 4-15,17-21 and 23-31 is/are pending in the application.  
 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.  
 5) Claim(s) 9-14,19,20 and 24-27 is/are allowed.  
 6) Claim(s) 4-8,15,17,18,21-23 and 28-31 is/are rejected.  
 7) Claim(s) \_\_\_\_\_ is/are objected to.  
 8) Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) The specification is objected to by the Examiner.  
 10) The drawing(s) filed on 28 February 2002 is/are: a) accepted or b) objected to by the Examiner.  
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).  
 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
 a) All    b) Some \* c) None of:  
 1. Certified copies of the priority documents have been received.  
 2. Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

- |  |   |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892)   | 4) <input type="checkbox"/> Interview Summary (PTO-413)                     |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                                   | Paper No(s)/Mail Date. _____  |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
|  | 6) <input type="checkbox"/> Other: _____                                    |

## **DETAILED ACTION**

1. Applicants' amendment filed on 2/11/04 has been received and entered in the case.

Claims 4-15, 17-21 and 23-31 are pending. The prior art rejections to claims 4-8, 15, 17-18, 21-23 and 28-31 are remained and repeated for the reasons set forth below. This action is FINAL.

### ***Claim Rejections - 35 USC § 102***

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 4-8, 15, 17-18 and 28-31 are rejected under 35 U.S.C. 102(b) as being anticipated by US Patent No. 6,111,445, issued to Zerbe et al.

As per claim 4, Zerbe discloses a circuit (Fig. 21), comprising:

a first node 2108 capable to provide a variable first voltage JX;

a second node 2109 capable to provide a variable second voltage JXB;

a first transistor 2316, coupled to the first node (at the drain), having a first gate for providing a first current (through transistor 2316) responsive to a first control voltage (the voltage at the gate of 2316) being applied to the first gate;

a second transistor 2318, coupled to the second node 2109 (at the drain), having a second gate for providing a second current responsive to a second control voltage being applied to the second gate;

a first control circuit (2313, 2312, 2315), coupled to the first gate and the second node 2109 (as shown), for providing the first control voltage responsive to the variable second voltage JXB (the first control voltage is provided at the gate of 2316 responsive to the second variable voltage JXB); and,

a second control circuit (2314, 2311, 2317), coupled to the second gate and the first node 2108 (as shown), for providing the second control voltage (at the gate of transistor 2318) responsive to the first variable voltage JX (the second control voltage is provided at the gate of 2318 responsive to the first variable voltage JX).

wherein the circuit further comprises:

a third transistor 2311, coupled to the first node (at the gate), having a third gate coupled to the first node (2108), for providing a third current (the current flows through transistor 2108) responsive to the first variable voltage JX; and,

a fourth transistor 2312, coupled to the second node (at the gate), having a having a fourth gate coupled to the second node (as shown), for providing a fourth current (the current flows through transistor 2312) responsive to the second variable voltage JXB.

As per claim 5, the recited limitation is met because they are current mirrors.

As per claim 6, since nodes 2108 and 2109 can receive any signal which includes signal from a clock signal, the recited limitation is met.

As per claim 7, the recited limitation is met because the circuit of claim 6 clearly can receive the clock signal has an amplitude of greater than approximately 400 mv.

As per claim 8, the recited limitation is merely an intended use and is met since the Zerbe circuit can be used for this purpose.

As per claim 15, this claim is rejected for the same reasons noted in claim 4.

As per claims 17-18, these claims are rejected for the same reasons noted in claims 5 and 8, respectively.

As per claim 28, this claim is merely a method to operate the circuit having elements and connections discussed in claim 4 above, since Zerbe teaches the circuit, he inherently teaches the recited method.

As per claims 29-31, these claims are rejected for the same reasons noted in claims 4-5 and 8, respectively.

### ***Claim Rejections - 35 USC § 103***

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

- (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 21-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 6,111,445, issued to Zerbe et al.

As per claim 21, Zerbe discloses a load circuit (Fig. 21) in a phase interpolator circuit (Fig. 5) wherein the load circuit includes elements discussed in claim 4. Zerbe further discloses that his interpolator circuit is used in a DLL or PLL circuit (column 1, lines 15-16).

Zerbe does not explicitly disclose that the interpolator circuit is in a receive circuit wherein the receive circuit is coupled to a transmit circuit as called for in the claim.

The examiner takes Official Notice the fact that in a memory system, a receiver circuit coupled to a transmit circuit to receive the signal from the transmit circuit is old and well-known in the art. Specific example would be the transmit circuit is a memory controller which exists in every computer system which transmit data and control signals to control and access data in the memory modules and the receiver circuit includes a PLL or DLL circuit.

It would have been obvious to one skilled in the art at the time of the invention was made to include the Zerbe's interpolator circuit in the PLL circuit in the receiver circuit.

The motivation and /or suggestion for doing so would have been obvious since by incorporating the Zerbe's interpolator circuit, noise immunity could be improved (column 1, lines 45). Therefore, it would have been obvious to include the interpolator circuit taught by Zerbe in a conventional receiver circuit to obtain the invention specified in the claim.

As per claims 22-23, these claims are rejected for the same reasons noted in claims 4-5, respectively.

#### ***Response to Arguments***

4.     Applicant's arguments filed on 2/11/04 have been fully considered but they are not persuasive.

Regarding the argument the examiner using the same transistors 2311 and 2312 for two distinctly claimed elements.

The applicants are requested to review the antecedent basis in the disclosure for the recited first, second, third, fourth transistors, the first and second control circuits used in claim 4 to see why the argument is not persuasive. As the applicants are well-aware, claim must be interpreted in light of the disclosure, not in vacuum. In the instant present invention, the disclosure teaches in Fig. 3, the first control circuit includes transistors 303, 304, 308, 309, 314 and 315 (disclosure, page 9, lines 12-13), and the first transistor is 307, the second control circuit includes transistors 305, 306, 310, 311, 316 and 317 (disclosure, page 9, lines 30-31), and the second transistor is 312. The teaching clearly implies the same transistors 309 and 310 (the third and fourth transistors) are for two distinctly elements. Therefore, the examiner's interpretation noted in the preceding rejection is consistent with what is taught in the applicants' disclosure.

The examiner further notes that it is easy to list the first control circuit includes only transistor 2313 and the second control circuit includes only transistor 2314 to leave transistors 2311 and 2312 for the third and fourth transistors, to meet the claim language. However, using this interpretation, the claim should be rejected under 112, second paragraph for failing to particularly point out the structural relationship between the first control circuit and the fourth transistor. Note that the language "the fourth transistor coupled to the second variable voltage and the first control circuit coupled to the second variable voltage" does not satisfy the 112, second paragraph requirement which is to particularly point out the structural relationship between the first control circuit and the fourth transistor if they are seen as distinctly claimed elements.

Regarding the argument the examiner has not shown where the reference teaches “obtaining a clock signal” and “applying a first voltage from the clock signal to a first transistor ...” regarding claim 28, and the examiner has the burden of showing with particularity where and how these claimed method are taught by the reference.

The examiner notes that it has been a common practice for an application having the combination of apparatus and method claims that if the claimed apparatus is anticipated by the reference, the method claim is also anticipated. The argument provides grounds for restriction requirements and the restriction requirements will be invoked later if needed to moot the argument regarding this matter.

***Allowable Subject Matter***

5. Claims 9-14, 19-20, 24-27 are allowed for the reasons noted in the previous Office Action.

***Conclusion***

6. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37

Art Unit: 2816

CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Minh Nguyen whose telephone number is 571-272-1748. The examiner can normally be reached on Monday, Tuesday, Thursday, Friday 7:00-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 571-272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

 3/3/04

Minh Nguyen  
Primary Examiner  
Art Unit 2816